FEATURES

- Low Power Consumption

- Thin, Lightweight Design Permits Easy Installation in a Variety of Equipment

- General-Purpose CMOS:
  - The Unit can be Easily Interfaced to a Microcomputer with Common 4-Bit and 8-Bit Parallel Inputs and Outputs

- Built-In Character Generator ROM, RAM, and Display Data RAM:
  - Character Generator ROM – 160 Different 5×7 Dot Matrix Character Patterns
  - Character Generator RAM – Eight Different User-Programmed 5×7 Dot Matrix Patterns (Write Capability by Program)
  - Display Data RAM – 80×8 bits

- Extensive Instruction Set:
  - Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Character Blink, Cursor Shift, and Display Shift

- Operates From a Single 5 V Power Supply and Incorporates an LCD Panel Which Provides a Highly Stable Display Over a Wide Range of Temperatures

DESCRIPTION

The SHARP LM20211 Dot Matrix LCD Unit consists of a combination of a 5×7 dot 20-character 2-line dot matrix LCD panel, LCD driver, and controller LSI mounted on a single printed circuit board. Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the unit is capable of efficiently displaying the desired characters under microcomputer control.
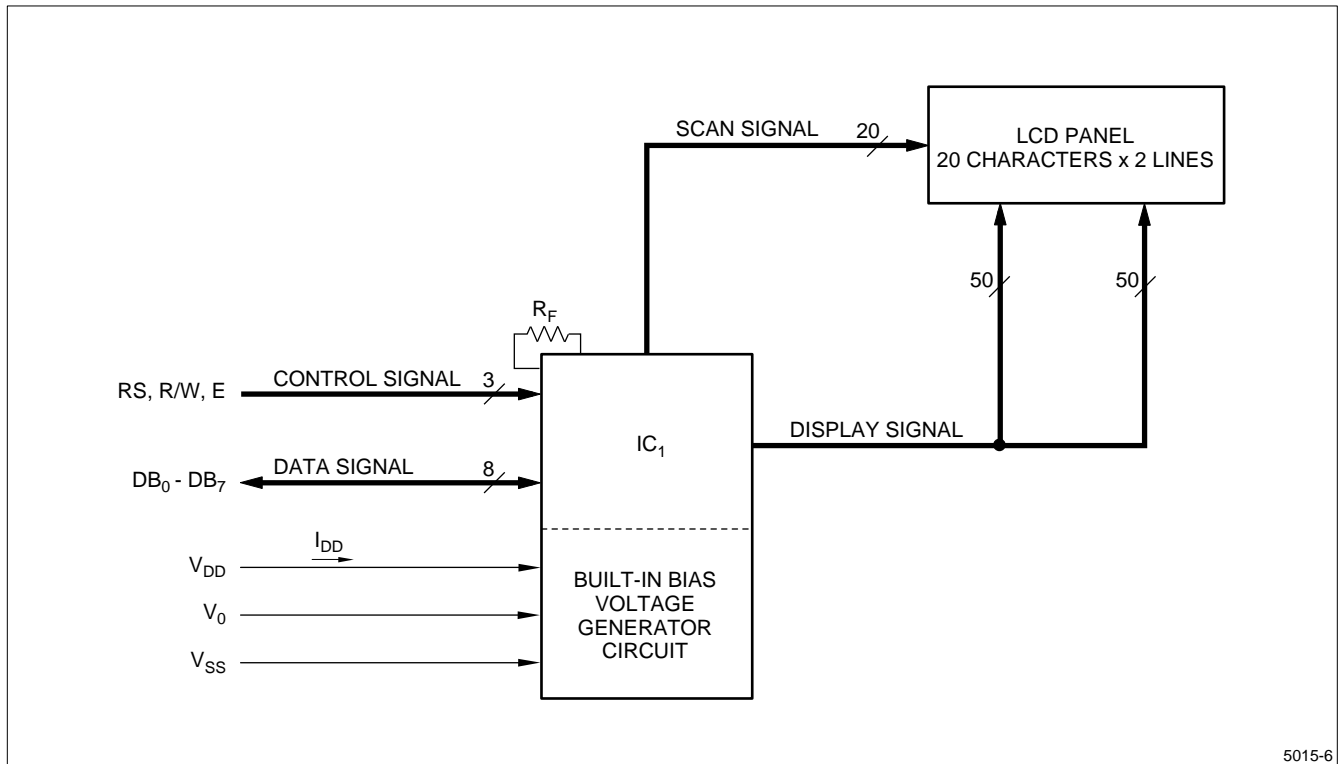
Figure 1. LM20211 Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT
Outline Dimensions	116 (W) $\times$ 32.5 (H) $\times$ 8 max (D)	mm
Active Area	88 (W) $\times$ 17.5 (H)	mm
Display Format	20 characters $\times$ 2 lines	–
Character Format	5 $\times$ 7 dots, with cusor	–
Character Size	3.05 (W) $\times$ 4.3 (H) (5 $\times$ 7 dots)	mm
Dot Size	0.55 (W) $\times$ 0.55 (H)	mm
Dot Spacing	0.075	mm
Character Color	Dark blue	–
Backlight Color	White	–
Weight	Approximately 25	g

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
V_{DD} - V_{SS}	Supply Voltage (Logic)	–0.3	+7.0	V	–
V_O - V_{SS}	Supply Voltage (LCD Drive)	0	+6.5	V	VDD > V_O
V_{IN}	Input Voltage (LCD Drive)	–0.3	V_{DD} +0.3	V	–
Tstg	Storage Temperature	–25	+70	°C	–
Topr	Operating Temperature	0	+50	°C	–

ELECTRICAL CHARACTERISTICS (t_A = 25°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE
$V_{DD} - V_{SS}$	Supply Voltage (Logic)		4.75	5.0	5.25	V	–
$V_O - V_{SS}$	Supply Voltage (LCD Drive)		–	0.4	–	V	V_{DD} = 5.0 V
V_{IL}	Input Voltage	'L'	–	–	0.6	V	–
V_{IH}		'H'	2.2	–	–	V	–
V_{OL}	Output Voltage	'L'	–	–	0.4	V	I_{OL} = 1.6 mA
V_{OH}		'H'	2.4	–	–	V	I_{OH} = −0.205 mA
I_{IL}	Input Leakage Current		-1	–	1	µA	–
f_{OSC}	Internal Oscillating Frequency		175	250	350	kHz	–
I_{DD}	Supply Current		–	0.6	1	mA	V_{DD} = 5.0 V
P_D	Power Dissipation		–	3	5	mW	V_O = 0 V

INTERFACE TIMING (V_{DD} = 5.0 V ±5%, t_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{CYCE}	Enable Cycle Time	500	–	–	ns
PW_{EH}	Enable Pulse Width	220	–	–	ns
t_{ER}, t_{EF}	Enable Rise/Fall Time	–	–	20	ns
t_{AS}	R_S, R/W Setup Time	40	–	–	ns
t_{AH}	Address Hold Time	10	–	–	ns
t_{DSW}	Data Setup Time	100	–	–	ns
t_{DDR}	Data Delay Time	–	–	150	ns
t_H	Data Hold Time (Write)	10	–	–	ns
t_{DHR}	Data Hold Time (Read)	20	–	–	ns

WRITE OPERATION

READ OPERATION
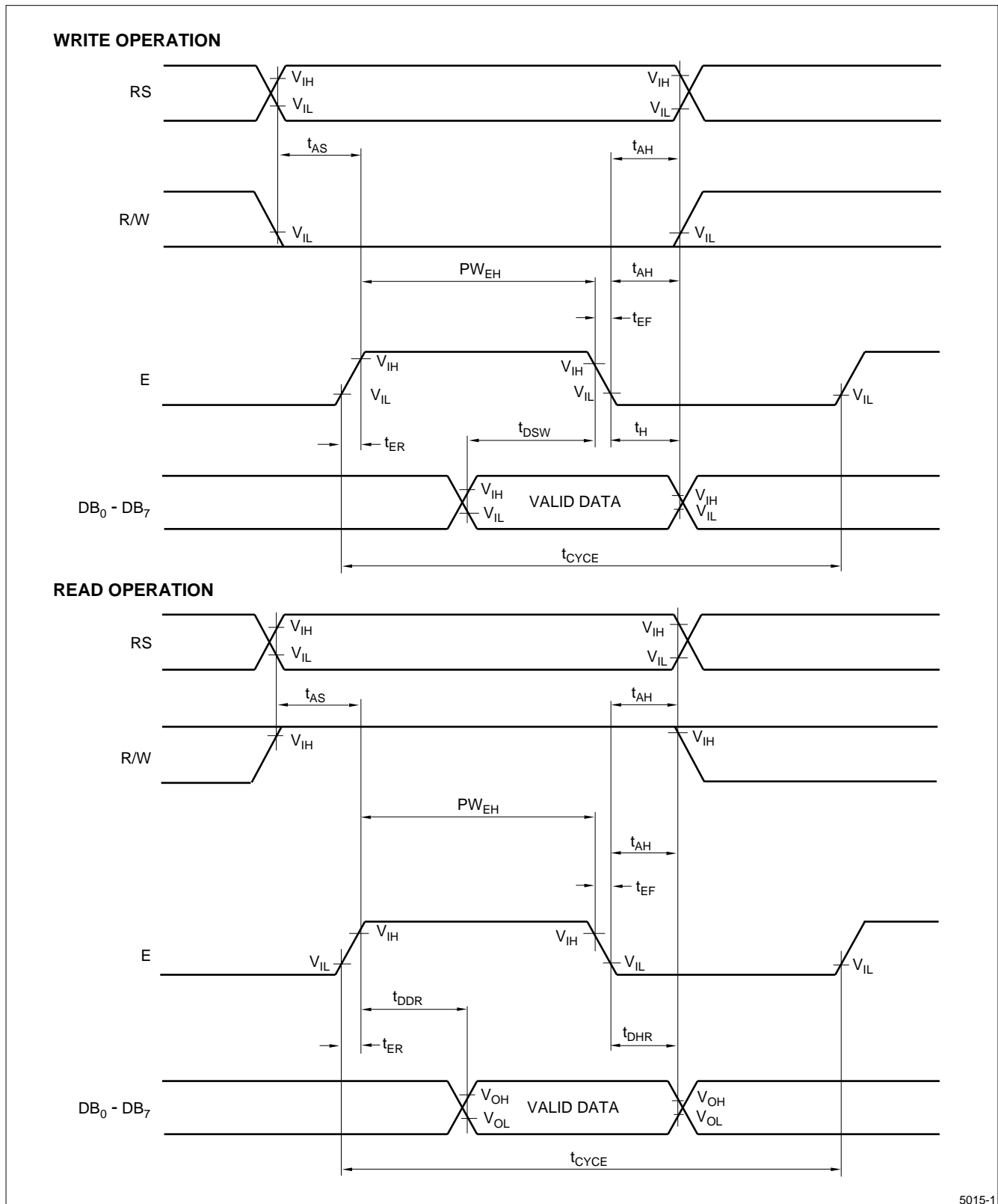
Figure 2. Interface Timing Chart

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PIN CONNECTIONS

PIN NUMBER	SYMBOL	DESCRIPTION	CONNECTION
1	V_{SS}	Ground Potential	GND: 0 V
2	V_{DD}	Power Supply	+5 V Power Supply
3	V_O	Contrast Adjustment Voltage	Adjust the contrast by supplying voltage from 0 V to 5 V
4	R_S	Register Select Pin	Control signal inputs
5	R/W	Read/Write Select Pin	
6	E	Enable Pin	
7	DB_0	Code I/O Data LSB	• Data bus signals • DB_7 may also be used to check the busy flag • DB_0 to DB_3 are not used when interfacing with a 4-bit micoprocessor
8	DB_1	Code I/O Data 2nd Bit	
9	DB_2	Code I/O Data 3rd Bit	
10	DB_3	Code I/O Data 4th Bit	
11	DB_4	Code I/O Data 5th Bit	
12	DB_5	Code I/O Data 6th Bit	
13	DB_6	Code I/O Data 7th Bit	
14	DB_7	Code I/O Data MSB	

OPTICAL CHARACTERISTICS ($V_{DD} - V_O$ = 4.0 V, t_A = 25°C)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
$\theta_2 - \theta_1$	Viewing Angle Range	$\phi = 0°$	$C_0 \geq 2.0$	30	–	–	degrees	1
θ_1		$\theta_1 < \theta_2$	$C_0 = 2.0$	–	–	15		
θ_2				40	–	–		
$\theta_2 - \theta_1$		$\phi = 90°$	$C_0 \geq 2.0$	30	–	–		
θ_1		$\theta_1 < \theta_2$	$C_0 = 2.0$	–	–	20		
θ_2				45	–	–		
C_0	Contrast Ratio	$\theta = 15°$		2.0	3.0	–	–	2
t_R	Response Speed – Rise	$\theta = 15°$		–	150	300	ms	3
t_D	Response Speed – Decay	$\theta = 15°$		–	200	400	ms	

NOTES:

1. The viewing angle range is defined as shown in Figure 3.
2. Contrast ratio is defined as follows:
   When input signal is applied to the unit to select (turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Figure 5.

   $$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non–select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

3. When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Figure 5. The response characteristics of the photodetector output are measured as shown in Figure 6.
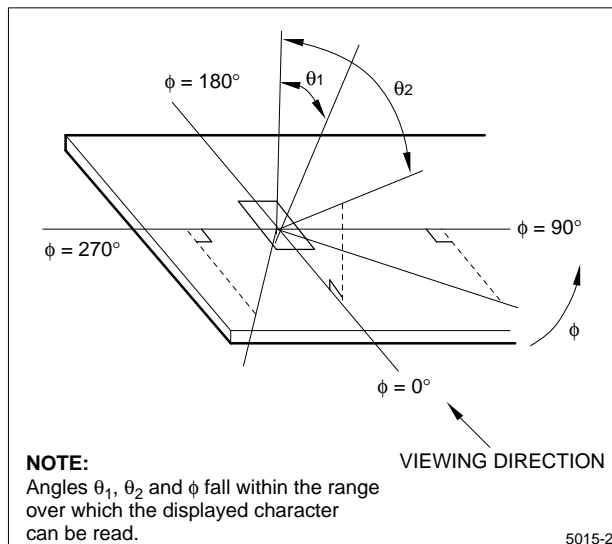
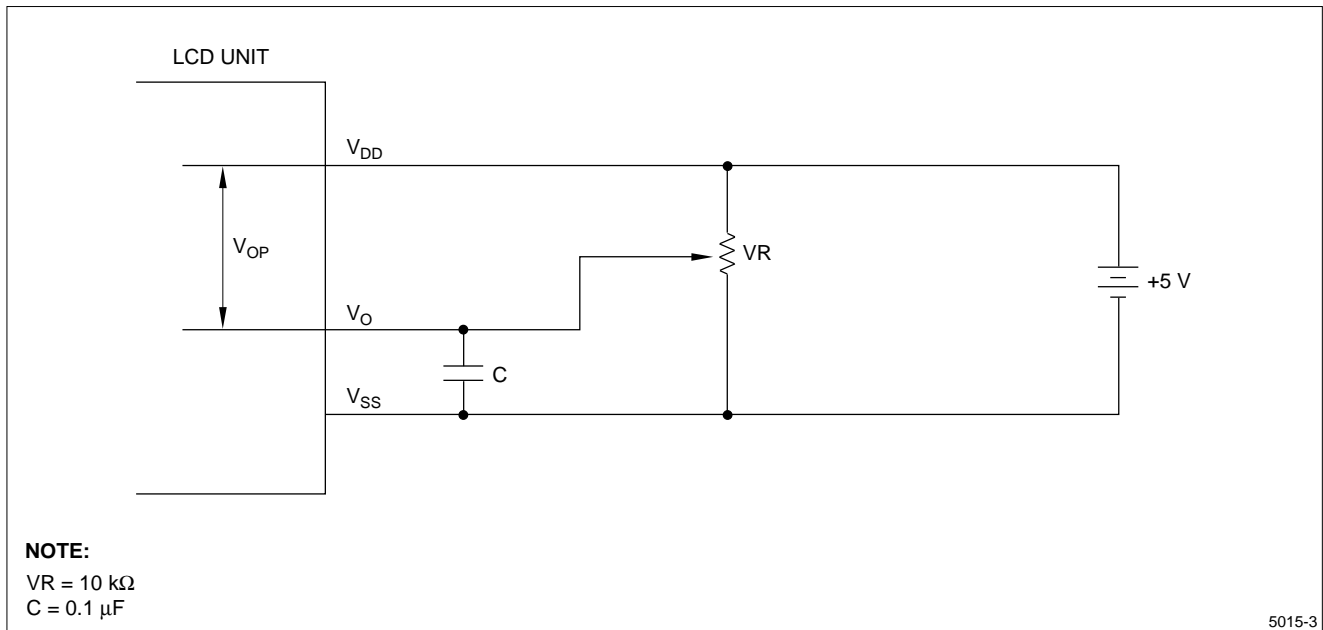
Figure 3. Definition of Viewing Angle
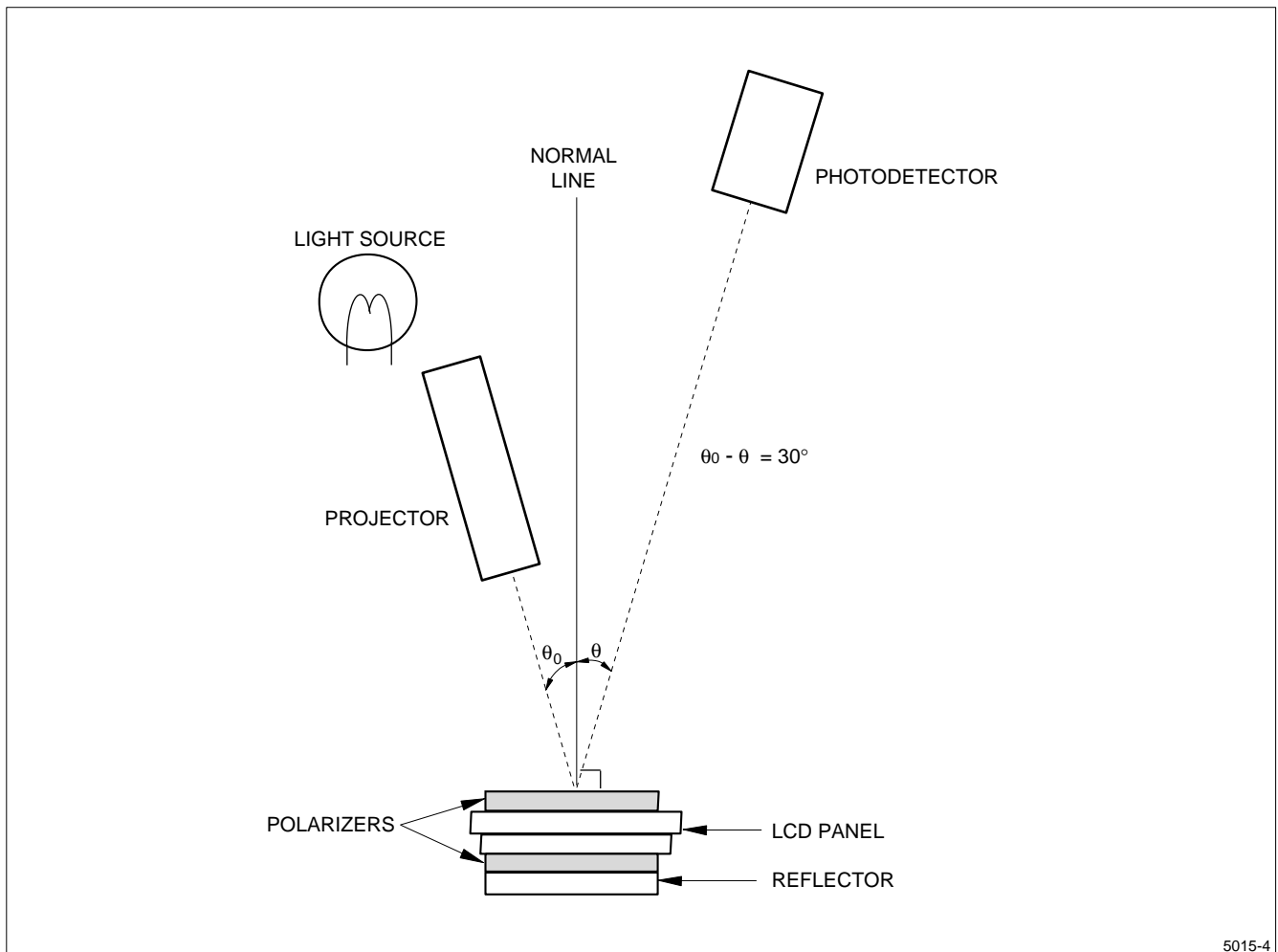
Figure 4. Contrast Adjust

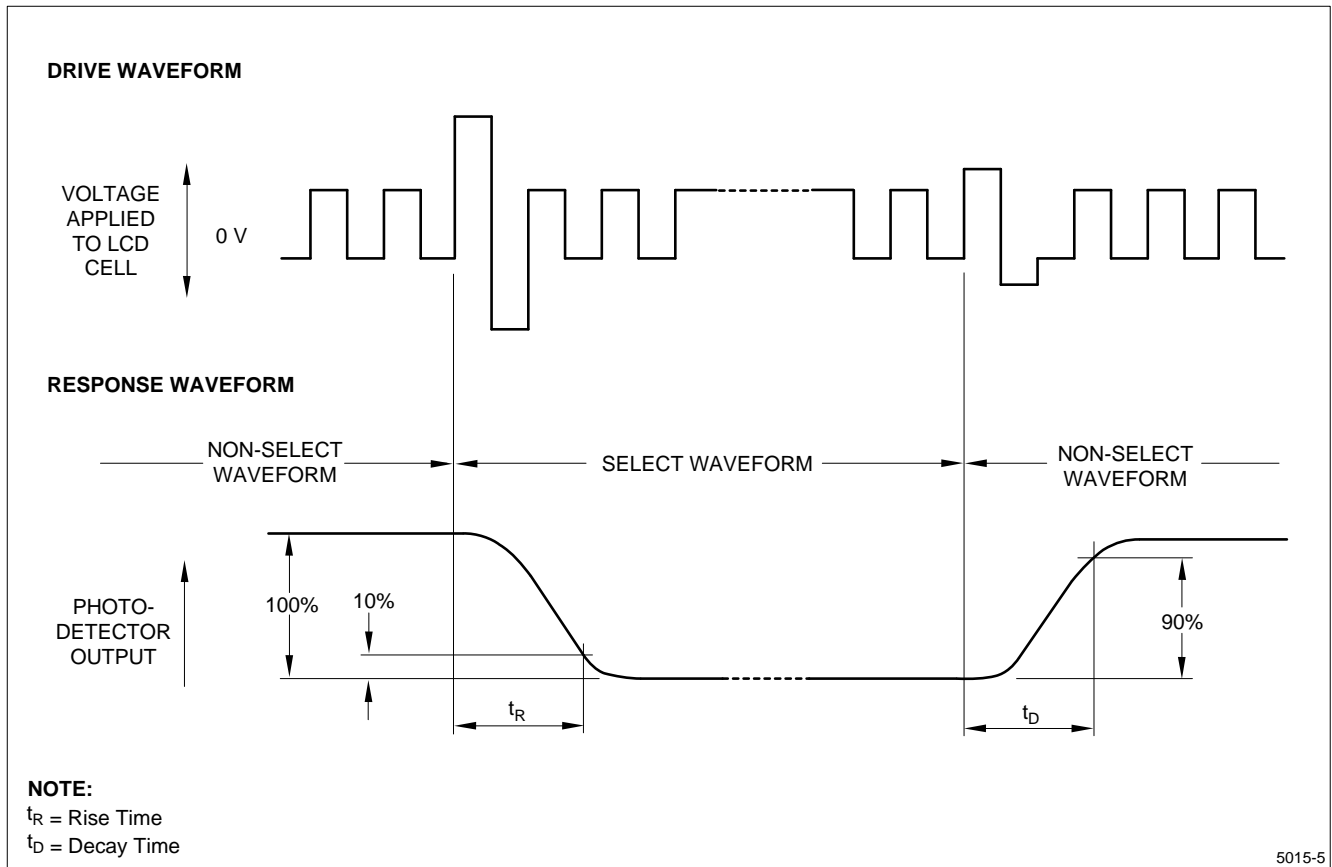**Figure 5. Optical Characteristics Test Method**

DRIVE WAVEFORM

VOLTAGE
APPLIED
TO LCD
CELL

0 V

RESPONSE WAVEFORM

NON-SELECT
WAVEFORM

SELECT WAVEFORM

NON-SELECT
WAVEFORM

PHOTO-
DETECTOR
OUTPUT

100%

10%

90%

t_R

t_D

NOTE:
t_R = Rise Time
t_D = Decay Time

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Figure 6. Definition of Response Time

PIN DESCRIPTION

V$_{DD}$ and V$_{SS}$ Pins

V$_{DD}$ and V$_{SS}$ pins are for the power supply. V$_{SS}$ pin is grounded, and V$_{DD}$ pin is supplied with +5 V. Each voltage necessary to drive LCD is generated in the unit.

RS Pin

The controller LSI contains two 8-bit registers: instructions register (IR) and data register (DR).

RS pin selects these registers. IR serves to store instruction codes for display clear, shift, etc. and address information for display data RAM (DD RAM), character generator RAM (CG RAM); DR serves to temporarily store data to be written into DD RAM and CG RAM.

'0': Instruction register (Write)
　　 Busy flag register; address counter (Read)

'1': Data register (Read/Write)

R/W Pin

Read or write selection signal pin.

'0': Write

'1': Read

E Pin

Data read or write operation enable signal pin.

DB$_0$ to DB$_7$ Pins

Tri-state bidirectional data bus pins. The bus allows data to be transmitted to or received from the external circuit. DB$_7$ serves also as busy flag output. When the unit is interfaced to a microcomputer with 4-bit parallel outputs, DB$_0$ to DB$_3$ pins are not used.

V$_0$ Pin

Viewing angle is varied and contrast is adjusted by changing input voltage between +5 V to 0 V by applying bias voltage to the LCD driver.

INSTRUCTION SET

INSTRUCTION	CODES										DESCRIPTION
	RS	R/W	DB$_7$	DB$_6$	DB$_5$	DB$_4$	DB$_3$	DB$_2$	DB$_1$	DB$_0$	
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area, restore display from shift, and load address counter with DD RAM address 00H.
Cursor Home	0	0	0	0	0	0	0	0	1	*	Restores display from shift and load address counter with DD RAM address 00H.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Decides which direction cursor is to be moved and whether display is to be shifted. The above operation is performed during a write or read cycle.
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Turns on and off display (D); cursor (C); blinks the character in the cursor position (B).
Cursor/ Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts the internal cursor and display while the contents of DD RAM remains unchanged.
Function Set	0	0	0	0	1	DL	1	0	*	*	Sets interface data length (DL).
CG RAM Address Set	0	0	0	1	A$_{CG}$						Sets CG RAM address (A$_{CG}$). The subsequent data is CG RAM data.
DD RAM Address Set	0	0	1	A$_{DD}$							Sets DD RAM address (A$_{DD}$). The subsequent data is DD RAM data.
Busy Flag/ Address Counter Read	0	1	BF	AC							Reads out busy flag (BF) denoting internal operation and address counter (AC).
CG RAM/ DD RAM Data Write	1	0	Write data								Writes data into DD RAM or CG RAM.
CG RAM/ DD RAM Data Read	1	1	Read data								Read data from DD RAM or CG RAM.

NOTES:

I/D = 1: Increment
S = 1: Display shift
D = 1: Display ON
C = 1: Cursor ON
B = 1: Character at cursor position blinks
I/D = 0: Decrement
S = 0: Display freeze
D = 0: Display OFF
C = 0: Cursor OFF

B = 0: Character at cursor position unblinks
S/C = 1: Display shift
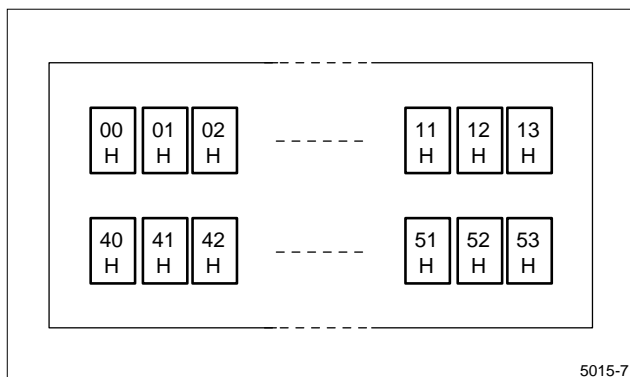R/L = 1: Right shift
DL = 1: 8 bits
BF = 1: During internal operation
S/C = 0: Internal cursor shift
R/L = 0: Left shift
DL = 0: 4 bits
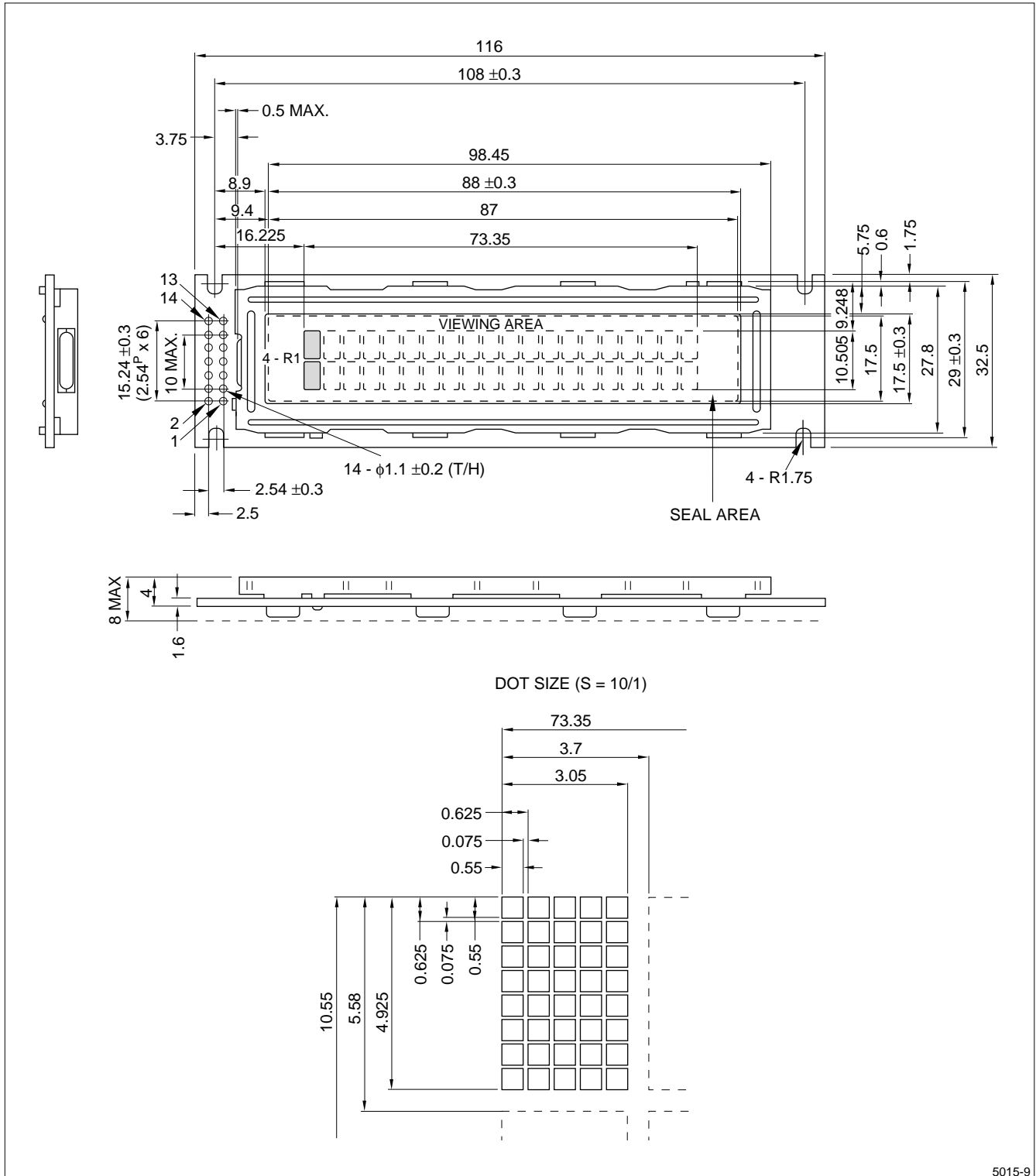BF = 0: End of internal operation

Figure 7. Display Address
(When the Display is Not Shifted)

HIGH-ORDER / LOW-ORDER 4 BIT	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxx0101	(6)												
xxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

NOTE: CG RAM is character generator RAM in which user-definable character patterns are stored.

Figure 8. Input Code Vs. Character Pattern

OUTLINE DIMENSIONS

DOT SIZE (S = 10/1)